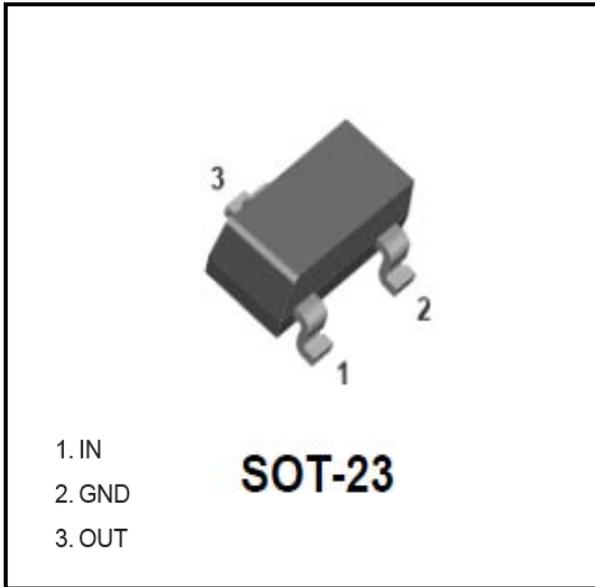


## NPN Digital Transistors (Built-in Resistors)



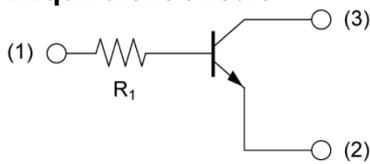
### Features

- Epoxy meets UL-94 V-0 flammability rating
- Moisture Sensitivity Level 1
- Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors
- Surface mount package ideally Suited for Automatic Insertion

### Mechanical Data

- **Package:** SOT-23
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102
- **Marking:** 03

### ■Equivalent circuit



- (1) BASE  
(2) EMITTER  
(3) COLLECTOR

### ■Maximum Ratings (Ta=25°C Unless otherwise specified)

ITEM	SYMBOL	UNIT	CONDITIONS	VALUE
Collector-Emitter Voltage	$V_{CEO}$	V		50
Collector-Base Voltage	$V_{CBO}$	V		50
Emitter-Base Voltage	$V_{EBO}$	V		5
Collector Current	$I_C$	mA		100
Power Dissipation	$P_D$	mW		200
Junction Temperature	$T_J$	°C		-55 to +150
Storage Temperature	$T_{STG}$	°C		-55 to +150



# DTC143TCA

## ■ Electrical Characteristics (Ta=25°C unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Collector-base breakdown voltage	$V_{(BR)CBO}$	V	$I_C=50A$	50		
Collector-emitter breakdown voltage	$V_{(BR)CEO}$	V	$I_C=1mA$	50		
Emitter-base breakdown voltage	$V_{(BR)EBO}$	V	$I_E=50\mu A$	5		
Collector-base cut-off current	$I_{CBO}$	$\mu A$	$V_{CB}=50V$			0.5
Emitter-base cut-off current	$I_{EBO}$	$\mu A$	$V_{EB}=4V$			0.5
DC current gain	$h_{FE}$		$V_{CE}=5V, I_C=1mA$	100		600
Input resistance	$R_1$	k $\Omega$		3.29	4.7	6.11
Collector-emitter saturation voltage	$V_{CE(sat)}$	V	$I_C=5mA, I_B=0.25mA$			0.3
Transition frequency	$f_T$	MHz	$V_{CE}=10V, I_E=5mA, f=100MHz$		250	

## ■ Ordering Information (Example)

PREFERRED P/N	PACKING CODE	UNIT WEIGHT(g)	MINIMUM PACKAGE(pcs)	INNER BOX QUANTITY(pcs)	OUTER CARTON QUANTITY(pcs)	DELIVERY MODE
DTC143TCA	F2	Approximate 0.009	3000	30000	120000	7" reel

## ■ Thermal Characteristics (Typical)

PARAMETER	SYMBOL	UNIT	VALUE
Thermal resistance, junction-to-ambient	$R_{thJA}$ (1)	°C/W	625
Thermal resistance, junction-to-case	$R_{thJC}$ (1)	°C/W	500

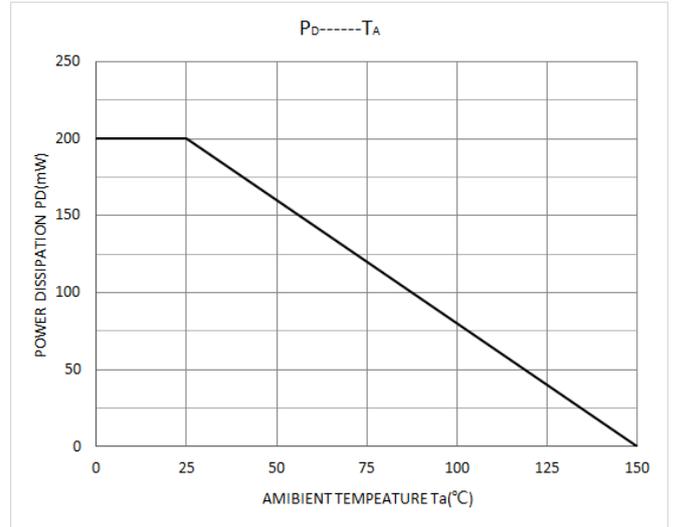
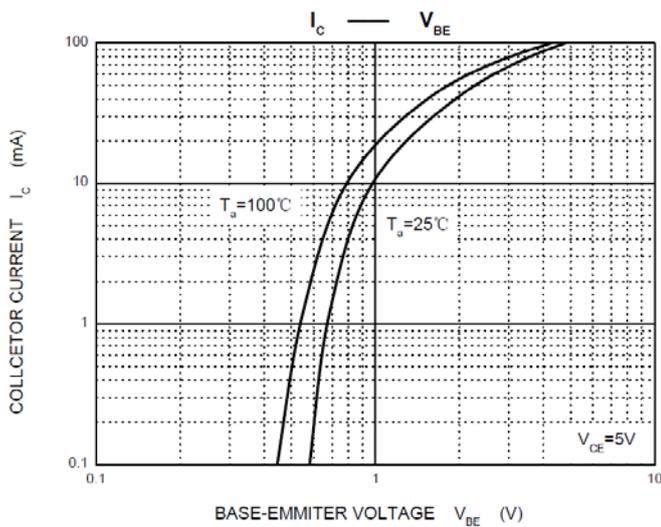
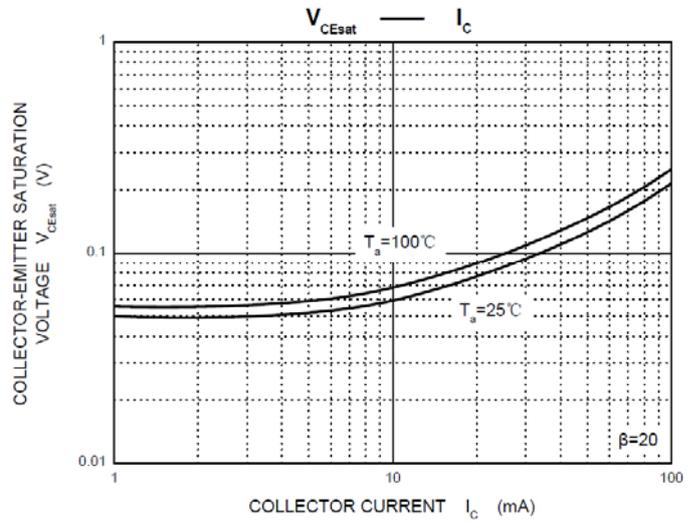
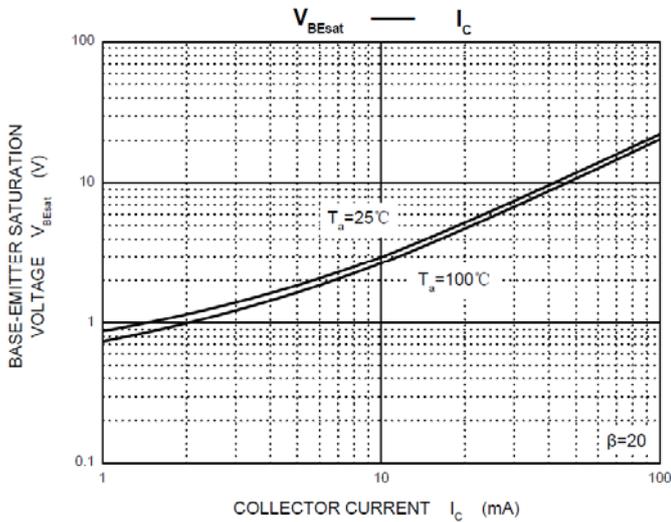
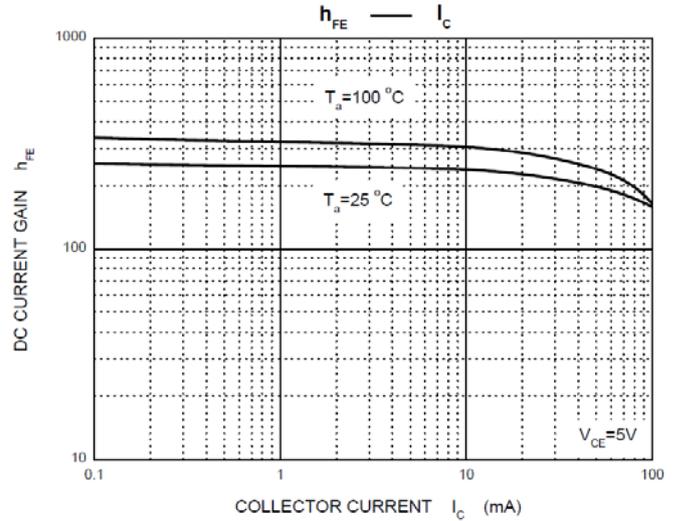
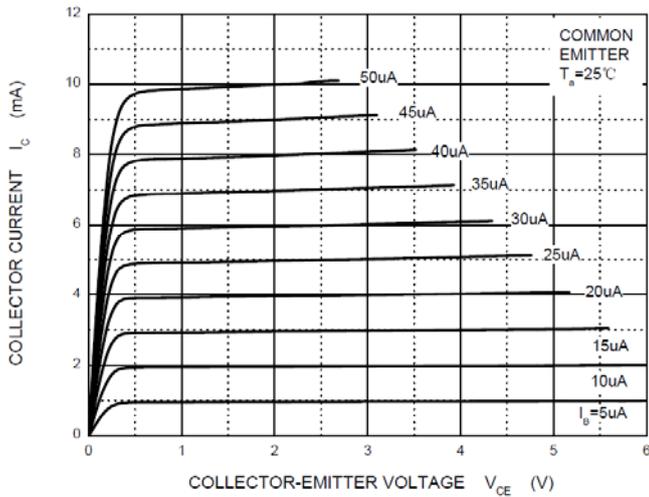
Note:1.Device mounted on PCB, single-sided copper, with standard footprint.



# DTC143TCA

## ■ Characteristics (Typical)

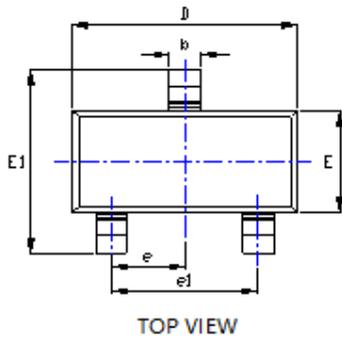
### Static Characteristic



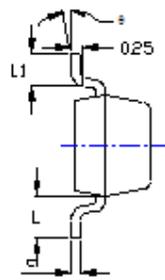


# DTC143TCA

## ■SOT-23 Package Outline Dimensions



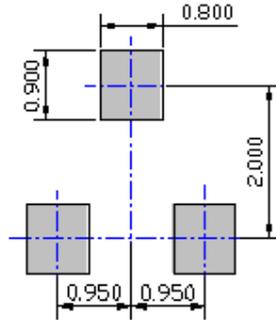
TOP VIEW



SIDE VIEW



SIDE VIEW



UNIT: mm

SUGGESTED SOLDER PAD LAYOUT

SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.045	0.900	1.150
A1	0.000	0.004	0.000	0.100
A2	0.035	0.041	0.900	1.050
b	0.012	0.020	0.300	0.500
c	0.004	0.008	0.100	0.200
D	0.110	0.118	2.800	3.000
E	0.047	0.055	1.200	1.400
E1	0.089	0.100	2.250	2.550
e	0.037TYP		0.950TYP	
e1	0.071	0.079	1.800	2.000
L	0.022REF		0.550REF	
L1	0.012	0.020	0.300	0.500
φ	0°	8°	0°	8°

NOTE:

1.PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.

2.TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.

3.THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:

1. All dimensions are in millimeters (mm) unless otherwise specified.

[所有尺寸均以毫米为单位，除非另有说明]

2. General tolerances:  $\pm 0.10\text{mm}$  unless otherwise specified.

[通用公差为 $\pm 0.10\text{mm}$ ，除非另有说明]

3. Dimensions and tolerances per ASME Y14.5M-2018.

[尺寸和公差遵循 ASME Y14.5M-2018 标准]

4.All dimensions shown are exclusive of burrs and gate residues. Burrs and gate vestiges shall not exceed 0.15 mm in maximum.

[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]

5.Dimension b does not include dambar protrusion of max 0.100 mm per side.

[尺寸b不包括单边最大0.100 MM的中筋凸出部分]

6.Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.

[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸]

7.Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.

[成型的管脚应为同一平面，共面性最大为0.1mm]

8. ★It is the key size.

[★ 标记为关键尺寸]



## DTC143TCA

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