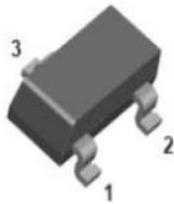
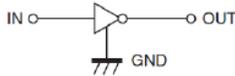
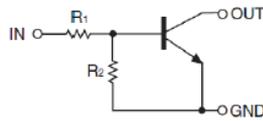


## NPN Digital Transistors (Built-in Resistors)



1. IN  
2. GND  
3. OUT

**SOT-323**

### Features

- Moisture sensitivity level 1
- Halogen free and RoHS compliant
- Surface mount package ideally suited for automatic insertion

### Application

- Signal amplification
- Switching circuit

### Mechanical data

- **Package:** SOT-323
- **Terminals:** Tin plated leads, solderable per J-STD-002 and JESD22-B102

### ■ Maximum Ratings ( $T_a=25^\circ\text{C}$ Unless otherwise specified)

Item	Symbol	Unit	Conditions	Value
Device marking code				235
Supply voltage	$V_{CC}$	V		50
Input voltage	$V_{IN}$	V		-10 to +30
Output current	$I_o$	mA		500
Power dissipation	$P_D$	mW		200
Junction temperature	$T_J$	$^\circ\text{C}$		-55 to +150
Storage temperature	$T_{STG}$	$^\circ\text{C}$		-55 to +150



# DDTC143EUA

RoHS  
COMPLIANT

## ■ Electrical Characteristics (Ta=25°C Unless otherwise specified)

Item	Symbol	Unit	Conditions	Min	Typ	Max
Input voltage	$V_{I(off)}$	V	$V_{CC}=5V, I_o=100\mu A$	0.5		
	$V_{I(on)}$	V	$V_o=0.3V, I_o=20mA$			3
Output voltage	$V_{O(on)}$	V	$I_o / I_i = 10mA / 0.5 mA$			0.3
Input current	$I_i$	mA	$V_i=5V$			1.8
Output current	$I_{O(off)}$	$\mu A$	$V_{CC}=50V, V_i=0$			0.5
DC current gain	$G_i$		$V_o=5V, I_o = 10mA$	30		
Input resistance	$R_1$	k $\Omega$		3.29	4.7	6.11
Resistance ratio	$R_2/R_1$			0.8	1	1.2
Transition frequency	$f_T$	MHz	$V_{CE}=10V, I_E=-50mA, f=100MHz$		200	

## ■ Thermal Characteristics

Parameter	Symbol	Unit	Value
Thermal resistance, junction-to-ambient	$R_{\theta J-A}^{(1)}$	$^{\circ}C/W$	625
Thermal resistance, junction-to-case	$R_{\theta J-C}^{(1)}$	$^{\circ}C/W$	500

Note:

(1) Device mounted on PCB, single-sided copper, with standard footprint

## ■ Ordering Information

Preferred P/N	Packing code	Unit weight(g)	Minimum package(pcs)	Inner box quantity(pcs)	Outer carton quantity(pcs)	Delivery mode
DDTC143EUA	F2	Approximate 0.005	3000	30000	120000	7" reel



■ Characteristics

Fig 1: Input Voltage (On) Characteristics

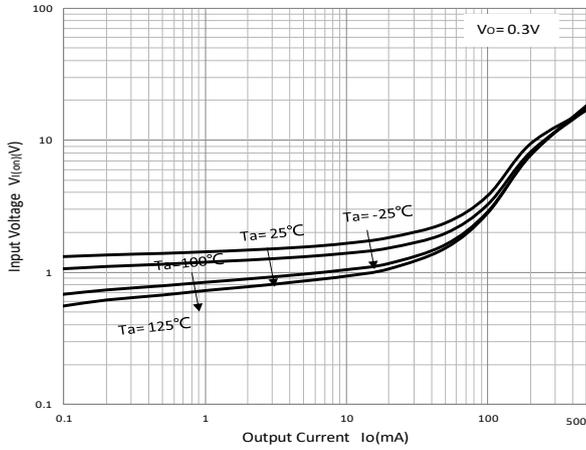


Fig 2: Input Voltage (Off) Characteristic

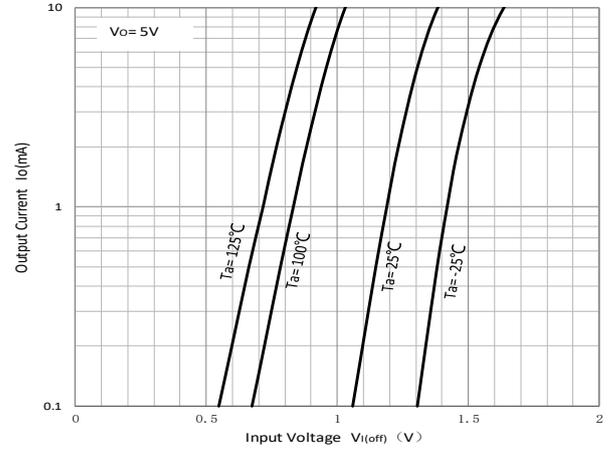


Fig 3: DC Current Gain Characteristics

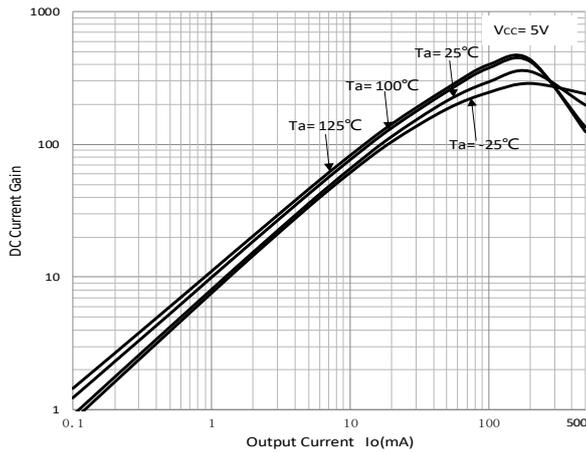


Fig 4: Output Voltage Characteristics

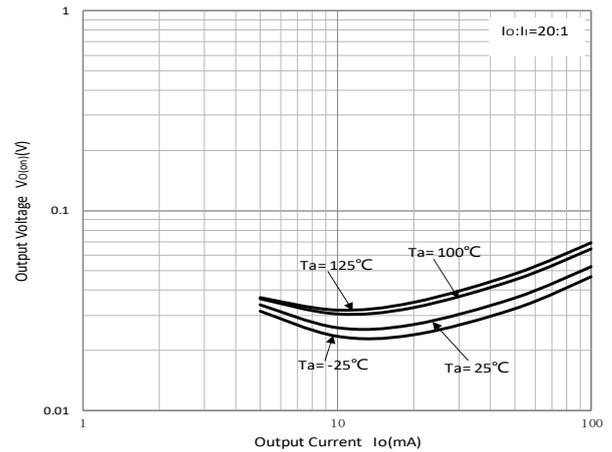
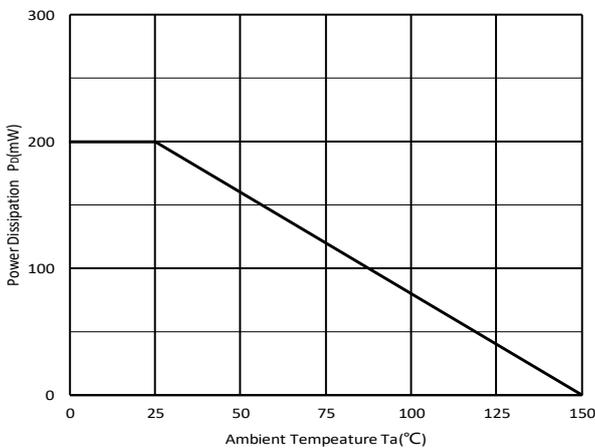
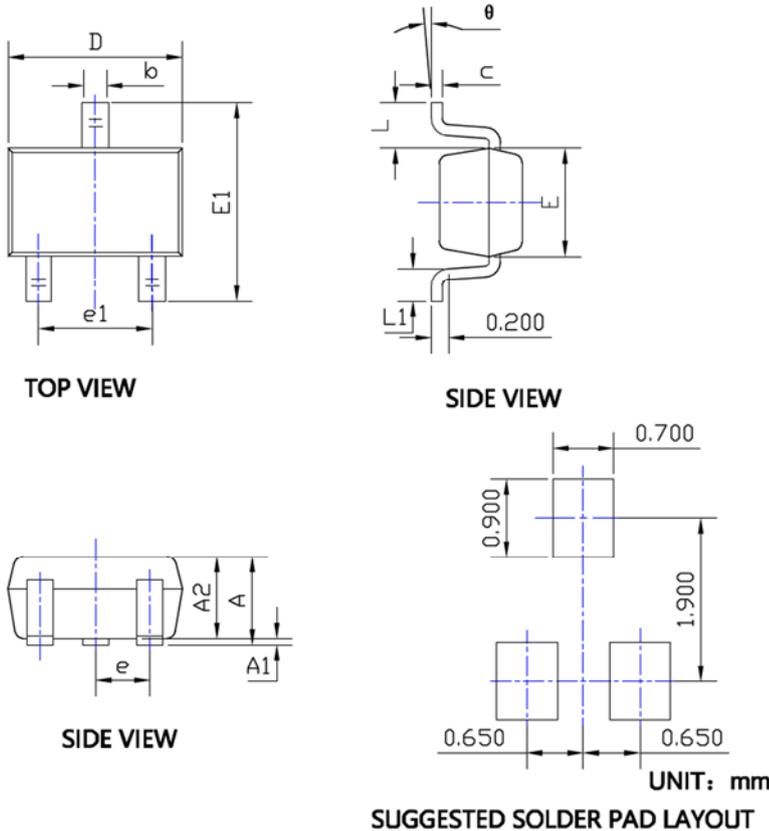


Fig 5:  $P_D$ - $T_a$  Curve



## ■ Outline Dimensions



SYMBOL	DIMENSIONS			
	INCHES		Millimeter	
	MIN.	MAX.	MIN.	MAX.
A	0.035	0.043	0.900	1.100
A1	0.000	0.004	0.000	0.100
A2	0.035	0.039	0.900	1.000
b	0.006	0.016	0.150	0.400
c	0.004	0.010	0.100	0.250
D	0.071	0.087	1.800	2.200
E	0.045	0.053	1.150	1.350
E1	0.085	0.096	2.150	2.450
e	0.026TYP		0.650TYP	
e1	0.047	0.055	1.200	1.400
L	0.021REF		0.525REF	
L1	0.010	0.018	0.260	0.460
θ	0°	8°	0°	8°

**NOTE:**  
 1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.  
 2. TOLERANCE 0.1mm UNLESS OTHERWISE SPECIFIED.  
 3. THE PAD LAYOUT IS FOR REFERENCE PURPOSES ONLY.

Note:

- All dimensions are in millimeters (mm) unless otherwise specified.  
[所有尺寸均以毫米为单位，除非另有说明]
- General tolerances:  $\pm 0.10\text{mm}$  unless otherwise specified.  
[通用公差为 $\pm 0.10\text{mm}$ ，除非另有说明]
- Dimensions and tolerances per ASME Y14.5M-2018.  
[尺寸和公差遵循 ASME Y14.5M-2018 标准]
- All dimensions shown are exclusive of burrs and gate residues.  
Burrs and gate vestiges shall not exceed 0.15 mm in maximum.  
[所有尺寸均不包括毛刺和浇口残留。毛刺与浇口残留的尺寸最大不得超过 0.15mm]
- Dimension b does not include dambar protrusion of max 0.100 mm per side.  
[尺寸b不包括单边最大0.100 MM的中筋凸出部分]
- Dimensions D and E are the overall extreme outer dimensions of the mold compound. These dimensions exclude mold flash, lead flash, protrusions and burrs but include the maximum allowable mold mismatch.  
[D和E是塑封体的外部极限尺寸，不包括包封溢料、内引线溢料、凸出部分以及胶体毛刺，但是包含了包封错位的最大尺寸]
- Formed leads shall be planar with respect to one another within a maximum of 0.076 mm relative to the seating plane.  
[成型的管脚应为同一平面，共面性最大为0.1mm]
- ★ It is the key size.  
[★ 标记为关键尺寸]



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